

Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 1207.P001C5	Application Number: Not yet assigned 10/492,880
	First Named Inventor: Benjamin S. Ting	
	Filing Date: Herewith 10/23/2003	

U.S. PATENT DOCUMENTS						
Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
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		Office ³	Number ⁴	Kind Code ⁵ (If known)					
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PCT		9208286			5/14/92				
EPO		0415542			3/6/91				
PCT		9410754			5/11/94				
UK		2180382			3/25/87				
Examiner Signature	James Sun bin					Date Considered	9-22-05		

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JSK		4,918,440	326/37	Furtek	4/17/90	
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Examiner Signature	<i>James P. Smith</i>	Date Considered	9-22-05
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		5,581,767	712/14	Katuski, et al.	12/3/96	
PR		6,160,420	326/41	Gamal	12/12/00	

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		Office ³ Code ⁵	Number ⁴	Kind (If known)				

Examiner Signature	<i>James P. Harris</i>	Date Considered	9-22-05
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 001207.P001C5	Application Number: 10/692,880 Not yet assigned
Examiner: Le, Don P.	First Named Inventor: Benjamin S. Ting	
Art Unit: 2819 Confirmation No.: 2347	Filing Date: Herewith 10/23/2003	

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
		*SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
		*ATMEL Field Programmable Arrays, AT 6000 Series, 1993, p. 1-16.	
		Altera Corporation Data Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	
		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
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		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5.	
		VIDAL, J. J., "Implementing Neural Nets with Programmable Logic," IEEE Transactions on Acoustic, Speech, and Signal Processing, Vol. 36, No. 7, July 1988, pp. 1180-1190.	
		LIU, D.L., et al., "Design of Large Embedded CMOS PLA's for Built-In Self-test," IEEE Transactions on Computed-Aided Design, Vol. 7, No. 1, January 1988, pp. 50-53.	
		SUN, Y., et al., "An Area Minimizer for Floorplans with L-Shaped Regions," 1992 International Conference on Computer Design, 1992 IEEE, pp. 383-386.	

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Examiner Signature	<i>James Sun</i>	Date Considered	9-22-05
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		<u>Minnick, R.C., "A Survey of Microcellular Research". Vol. 14, No. 2, 4/1967, pp. 203-241.</u>	
		<u>Cliff, et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", IEEE '93 pp. 7.3.1-7.3.5.</u>	
		<u>Xilinx, "The Programmable Gate Array Data Book", 1992.</u>	
		<u>Wescon '93, pp. 321-326.</u>	
		<u>Wescon '93, pp. 310-320.</u>	

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